Dr. A. Q. Khan Institute of Computer Science and

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Department of Computer Engineering

**Lab Report**

Computer Architecture Lab

Submitted To

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# HALF ADDER

## Objective:

To design and simulate a Half Adder circuit using ModelSim to perform binary addition of two input bits.

## Apparatus:

• ModelSim software  
• Computer system  
• Basic knowledge of digital logic gates

## Theory:

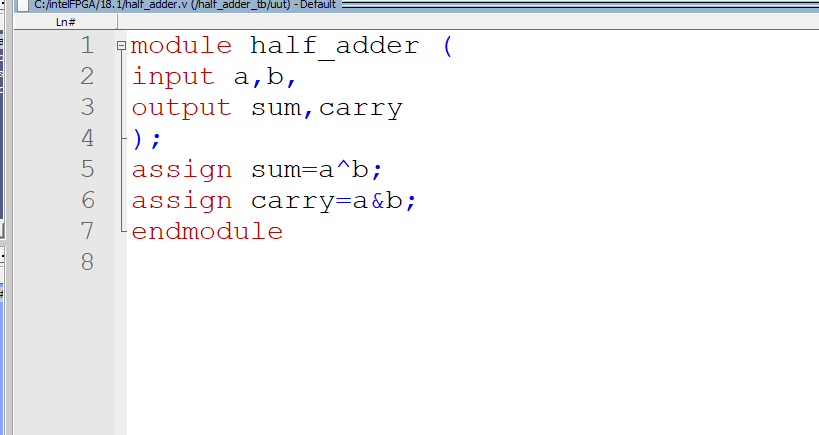
A Half Adder is a combinational logic circuit that performs the addition of two binary digits. It produces two outputs: SUM and CARRY. The SUM represents the least significant bit of the addition, while the CARRY represents the most significant bit.  
  
The logic expressions are as follows:  
SUM = A ⊕ B  
CARRY = A · B  
  
Where ⊕ denotes XOR operation and · denotes AND operation.

The truth table for the Half Adder is shown below:

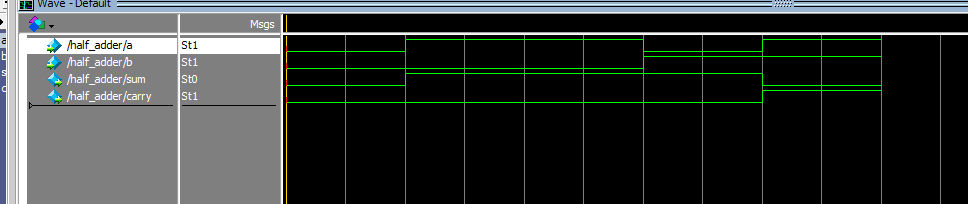
|  |  |  |
| --- | --- | --- |
| A | B | Outputs (SUM, CARRY) |
| 0 | 0 | 0, 0 |
| 0 | 1 | 1, 0 |
| 1 | 0 | 1, 0 |
| 1 | 1 | 0, 1 |

## Results:

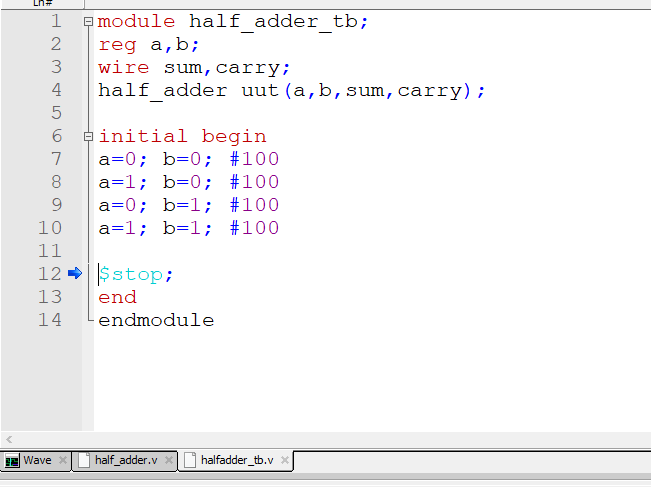
The Half Adder successfully performed the binary addition of two input bits. The simulated results matched the expected truth table outputs.



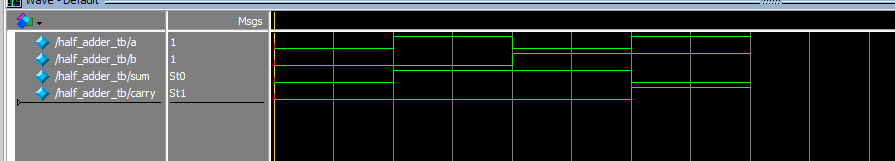
**Output**



# Test Bench:



**Output**



# FULL ADDER

## Objective:

To design and simulate a Full Adder circuit using ModelSim to perform binary addition of three input bits.

## Apparatus:

• ModelSim software  
• Computer system  
• Basic knowledge of digital logic gates

## Theory:

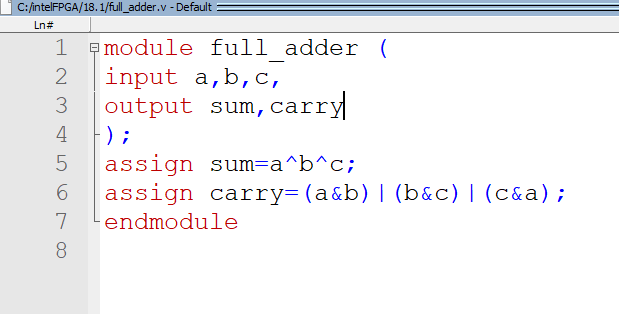
A Full Adder is a combinational circuit that performs the addition of three input bits: A, B, and Carry-in (Cin). It produces two outputs: SUM and Carry-out (Cout). The Full Adder can be constructed using two Half Adders and an OR gate.  
  
The logic expressions are:  
SUM = A ⊕ B ⊕ Cin  
CARRY = (A · B) + (B · Cin) + (A · Cin)  
  
Where ⊕ denotes XOR and · denotes AND operations.

The truth table for the Full Adder is shown below:

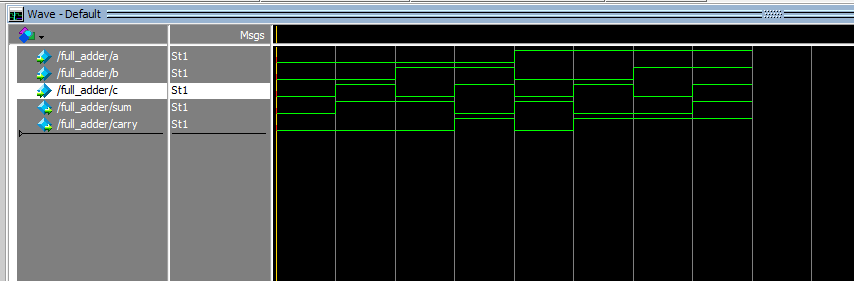
|  |  |  |  |
| --- | --- | --- | --- |
| A | B | Cin | Outputs (SUM, CARRY) |
| 0 | 0 | 0 | 0, 0 |
| 0 | 0 | 1 | 1, 0 |
| 0 | 1 | 0 | 1, 0 |
| 0 | 1 | 1 | 0, 1 |
| 1 | 0 | 0 | 1, 0 |
| 1 | 0 | 1 | 0, 1 |
| 1 | 1 | 0 | 0, 1 |
| 1 | 1 | 1 | 1, 1 |

## Results:

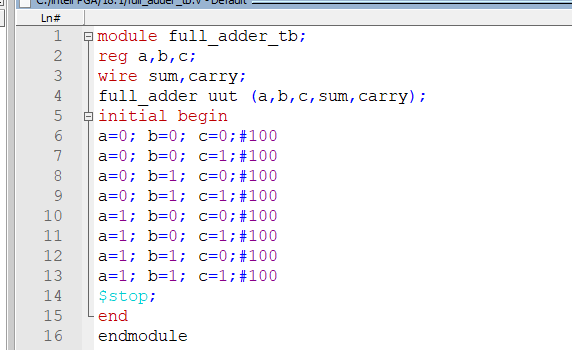
The Full Adder circuit successfully performed the addition of three binary inputs. Simulation results matched the expected truth table outputs, confirming correct operation.

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**Output**

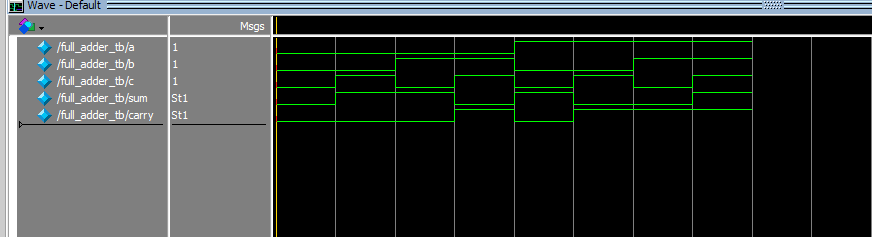
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**Test Bench:**

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**Output**

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